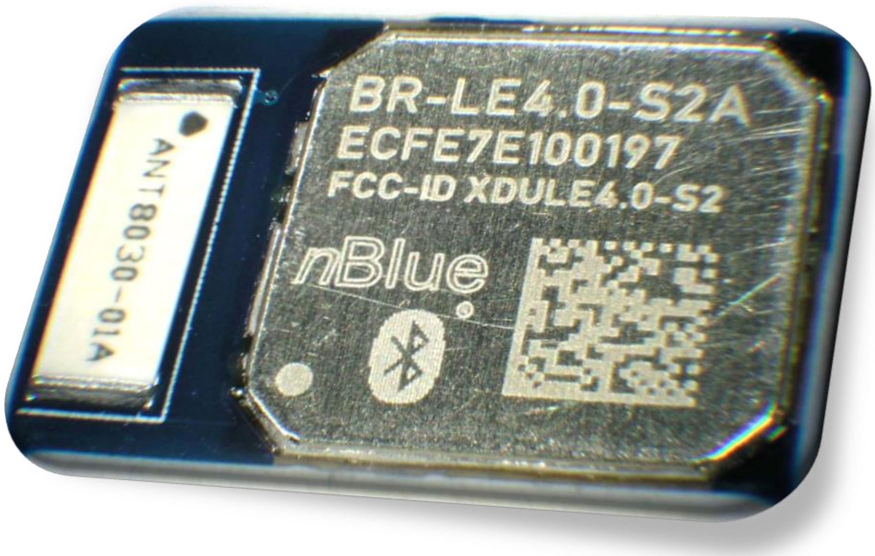
*n*Blue™ *Bluetooth*® 4.0 Module User's Guide



BR-LE4.0-S2A Single Mode Low Energy Module
(Actual Size Not Shown)

AT HOME. AT WORK. ON THE ROAD. USING BLUETOOTH WIRELESS TECHNOLOGY MEANS TOTAL FREEDOM FROM THE CONSTRAINTS AND CLUTTER OF WIRES IN YOUR LIFE.

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Revision History

Rev #	Date	Description
2.0	4/13/2012	**Initial Document** ▪ AT commands have been separated from the User's Guide into a separate AT.s Command Set document, which now includes commands for dual mode modules as well as single mode modules.
3.1	5/12/2012	▪ Added BR-LE4.0-D2 dual mode module hardware details
4.0	9/7/2012	▪ This document is now focused on hardware and independent of the AT.s Command Set, so the version has been bumped to 4.0.0 ▪ Updated Important Notes section with details on the bootloader ▪ Added BR-LE4.0-S3 single mode module hardware details ▪ Updated BR-LE4.0-S2 and BR-LE4.0-D2 module hardware details ▪ Added BR-LE4.0-D2 debugging information ▪ Added section on interface board ▪ Moved firmware update section to the *n*Blue Programmer User's Guide
4.1	2/8/2013	▪ Added D2 Current Consumption numbers ▪ Added more info on nBlue Programmer to Programming/Debugging section
4.2	3/13/2013	▪ Removed interface board section
4.3	1/28/2015	▪ Updated footprints to add JTAG and PCM pins for D2 modules

1 Introduction

"Our clients buy our products because they are reliable and easy to integrate, enabling them to quickly deploy cost-effective wireless solutions."

Mark J. Kramer – CEO of ***Blue*****Radios®**

1.1 Scope

This document along with the ***Blue*****Radios®** ***n*****Blue™** *Bluetooth*® low energy (BLE) evaluation kit was created to enable developers and integrators an opportunity to evaluate wireless networks using BLE technology. The goal is to make the transition to BLE as seamless and as easy as possible for our clients. This document will provide module hardware details.

1.2 Background

Bluetooth low energy was designed to enable the development of low complexity, low cost wireless devices that require minimal power consumption, such as sensors and watches. These devices typically transmit very small data packets at a time, while consuming as little power as possible. *Bluetooth* Version 4.0 specifies two types of implementation for BLE devices: single-mode and dual-mode. Single-mode chips implement the low energy specification and consume just a fraction of the power of classic *Bluetooth* (BR/EDR), allowing the short-range wireless standard to extend to coin cell battery applications. Dual mode chips combine low energy with the power of classic *Bluetooth* and are likely to become a standard feature in almost all new *Bluetooth* enabled cellular phones and computers (i.e., gateway devices).

The ***Blue*****Radios®** ***n*****Blue™** modules are *Bluetooth* Version 4.0 compliant. The modules are designed to be built into an embedded device and to provide a simple, reliable, and low cost API interface. The module is designed to integrate with a wide range of applications and platforms.

2 Important Notes – Please Read Prior To Continuing

2.1 Pin Voltage Levels

- The maximum voltage level on any pin should not exceed 3.6V. **The I/O is NOT 5V tolerant.**
- Applying VDD to a PIO set to an output may permanently damage the module.

2.2 Firmware Updates, nBoot Bootloader and IEEE Address

All *n*Blue modules come programmed with a bootloader (*n*Boot), to enable firmware updates via *n*Blue Programmer (*n*BP), and a *Blue*Radios IEEE address. These elements are stored in flash and can be accidentally erased using a debugger. Once they have been erased they cannot be reprogrammed by a client, it is a factory process only. When the *Blue*Radios IEEE address is erased, the TI IEEE address stored in ROM will be used.

To protect *Blue*Radios IP, any firmware distributed by *Blue*Radios or firmware built using libraries distributed by *Blue*Radios will not run without the presence of the nBoot bootloader. This means *Blue*Radios firmware will no longer run once the bootloader has been erased. At this point the module can only be programmed with custom firmware.

For security purposes, after the bootloader is programmed into BR-LE4.0-SX modules during production the debug interface is locked. In order to program a module using a CC Debugger it will then need to be unlocked, which will erase the entire flash including the module's bootloader and IEEE address, making it incapable of performing firmware updates using *n*BP. For this reason, single mode BR-LE4.0-SX firmware updates should only be performed using *n*BP, not a CC Debugger. Custom software can still be flashed using *n*BP, see the *n*Blue Programmer User's Guide for more information.

On BR-LE4.0-D2 modules the bootloader is locked separately from the program flash in the MSP430's BSL flash, so firmware can safely be loaded into the D2 through a debugger without erasing the bootloader.

2.3 Related Documents

- *n*Blue AT.s Command Set
- *n*Blue BR-EVAL-4.0-X2A Quick Start Guide
- *n*Blue Programmer User's Guide

3 Module Hardware Details

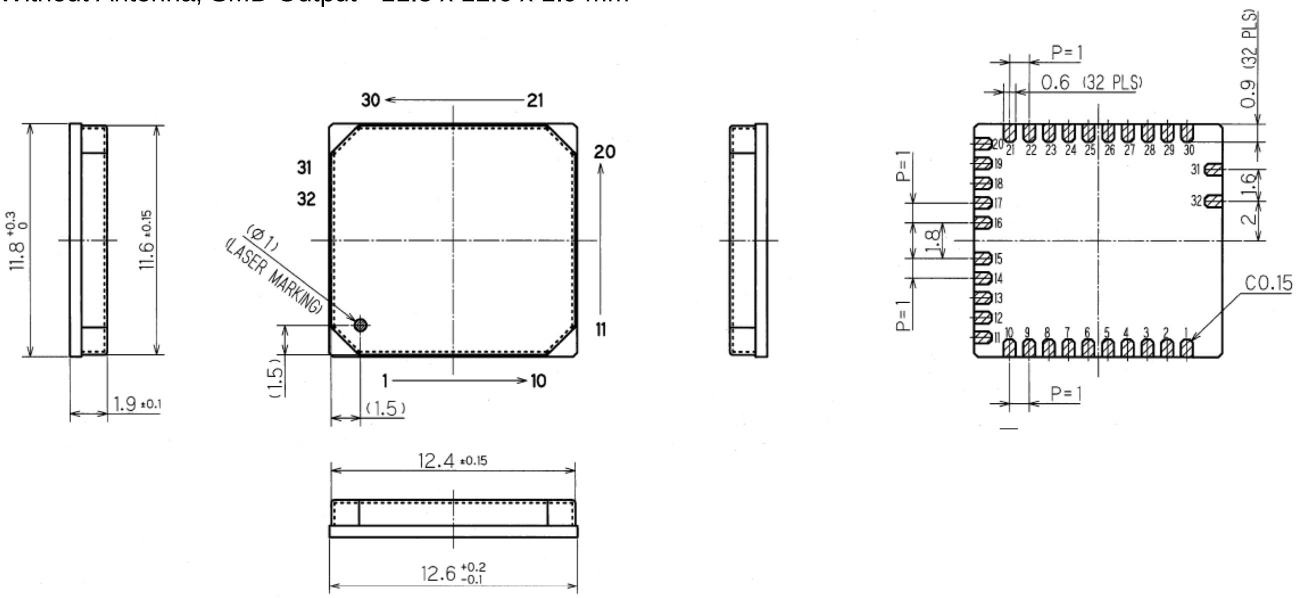
The *Blue*Radios *n*Blue low energy modules were designed to be as similar as possible to the legacy *Blue*Radios *Bluetooth* 2.0 C46 modules. The footprint of the *n*Blue modules is identical to the C46 module, with some small differences in the pinout.

3.1 Module Dimensions

The information in this section applies to all *n*Blue modules: BR-LE4.0-S2, BR-LE4.0-S3, and BR-LE4.0-D2.

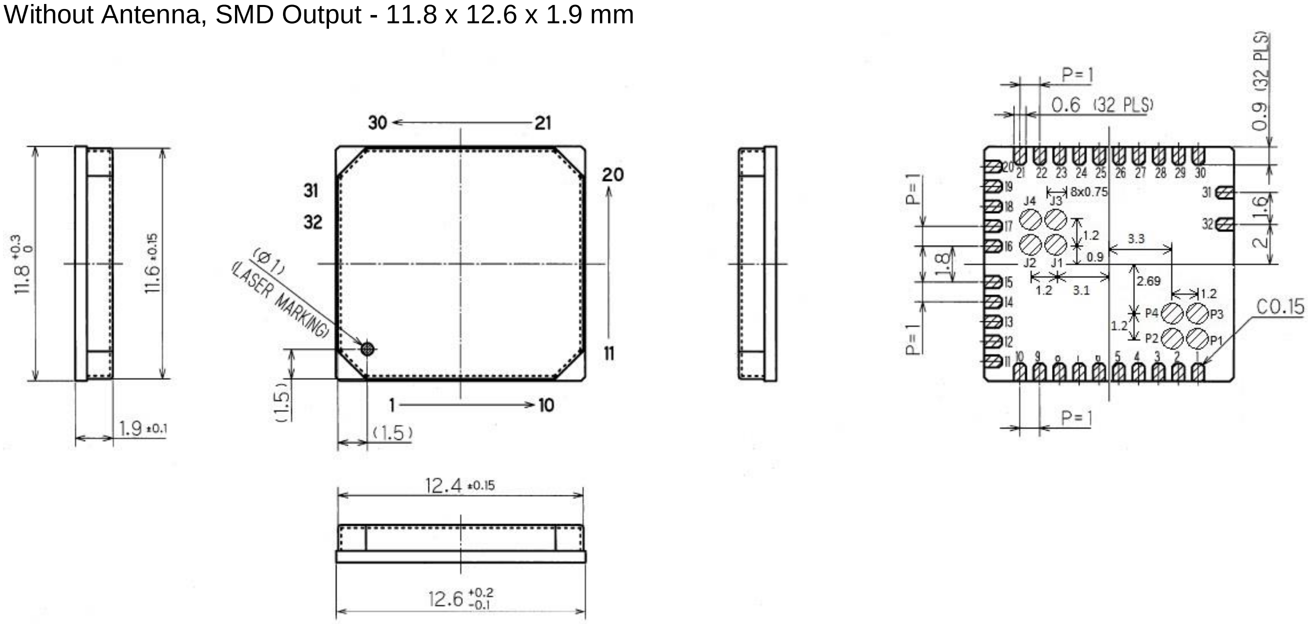
3.1.1 BR-LE4.0-S2N, BR-LE4.0-S3N (No Antenna)

Without Antenna, SMD Output - 11.8 x 12.6 x 1.9 mm



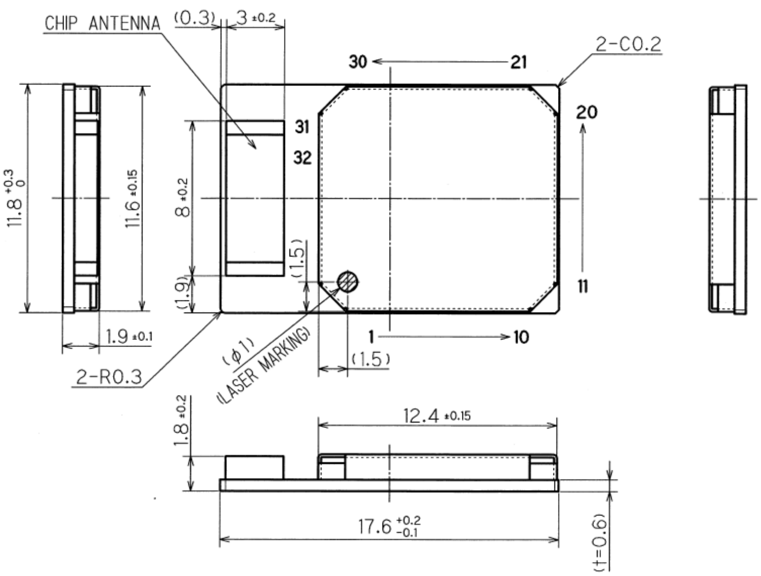
3.1.2 BR-LE4.0-D2N (No Antenna)

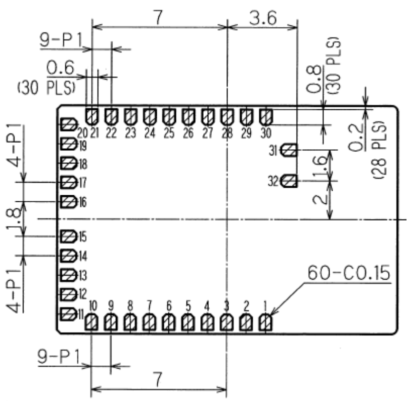
Without Antenna, SMD Output - 11.8 x 12.6 x 1.9 mm



3.1.3 BR-LE4.0-S2A, BR-LE4.0-S3A (With Antenna)

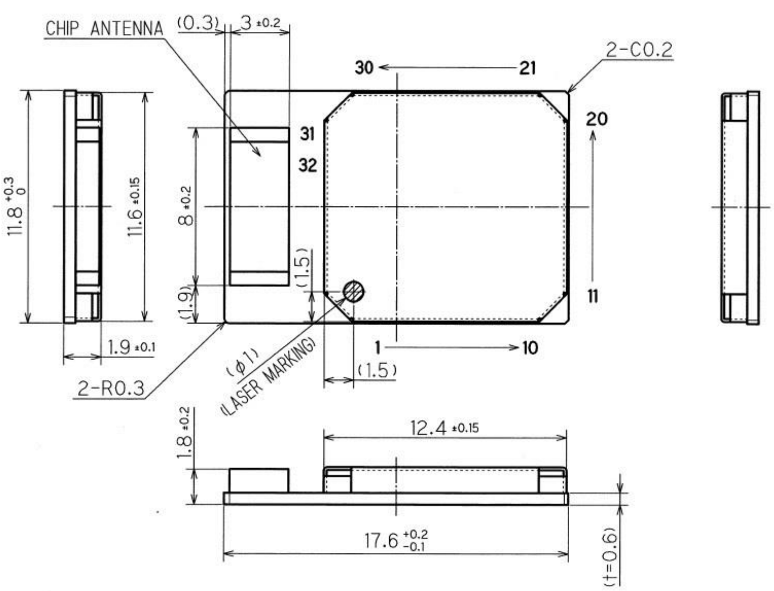
With 2 dBi TDK ATND8030-2R4-01 Antenna – 11.8 x 17.6 x 1.9 mm

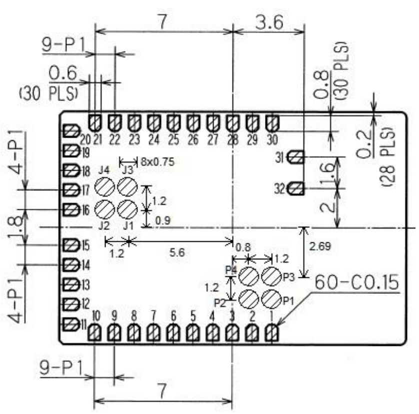




3.1.4 BR-LE4.0-D2A (With Antenna)

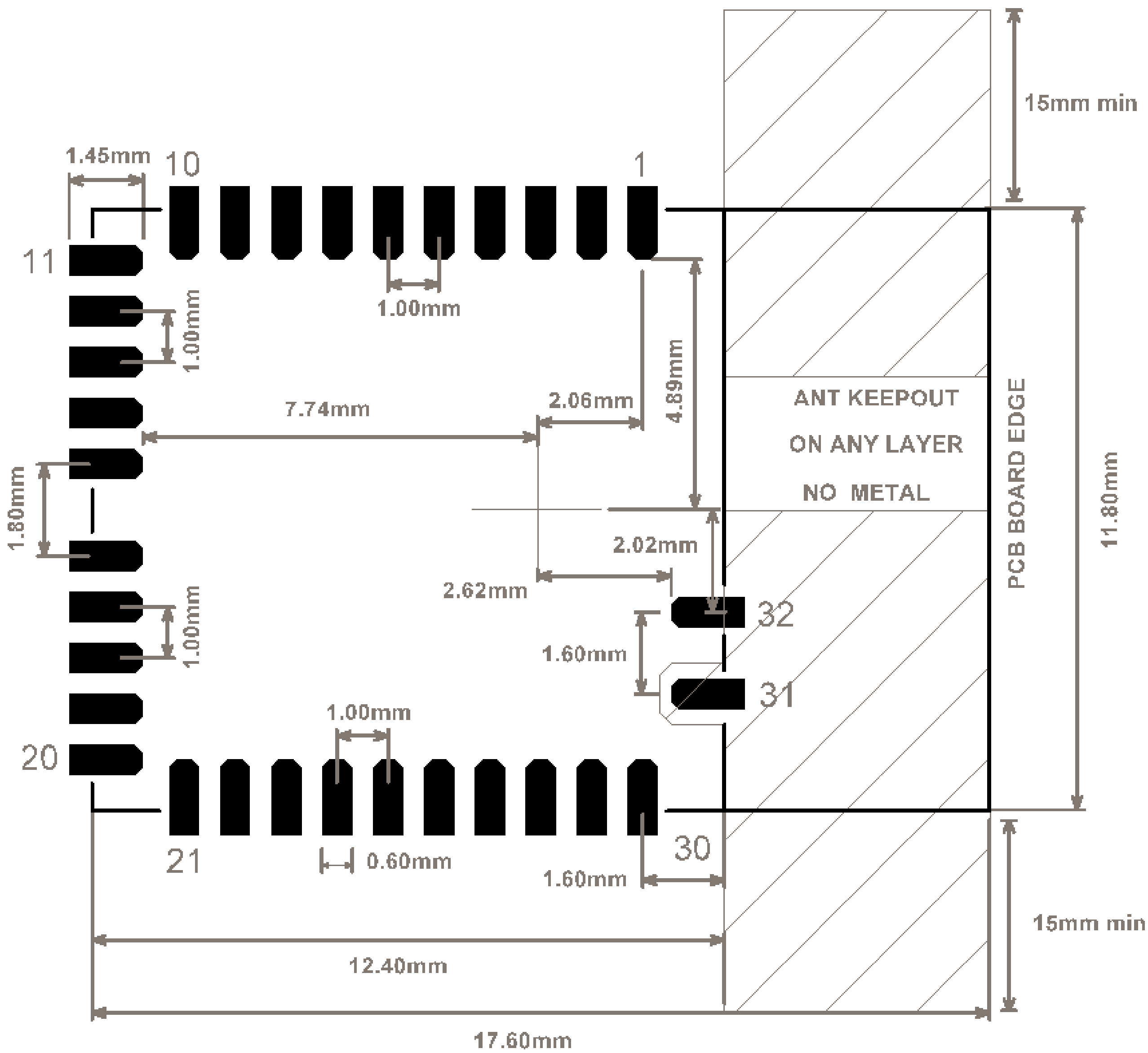
With 2 dBi TDK ATND8030-2R4-01 Antenna – 11.8 x 17.6 x 1.9 mm





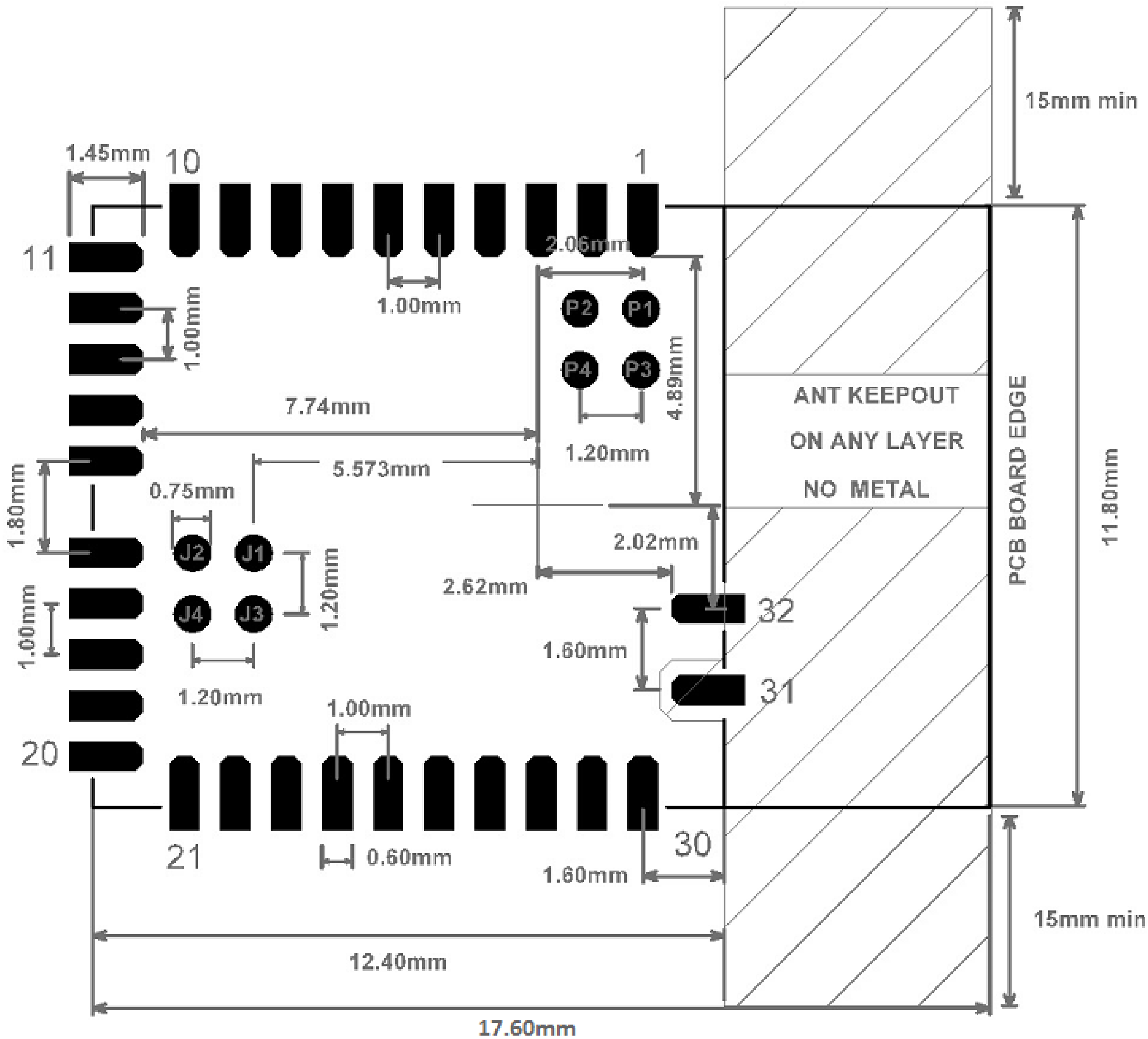
3.2 Module Standard Land Dimensions

3.2.1 BR-LE4.0-S2A, BR-LE4.0-S3A (With Antenna)



Note: The module requires an RF ground plane on the rest of the Printed Circuit Board (PCB) area. This can be located on any layer of the PCB. Extend the RF ground plane parallel to module pins 31 and 32 the entire length of your board. Connect all ground pins and do not notch the ground plane around the module. Bottom of module is grounded so be careful of vias or conductive traces located under the modules that are not soldered masked to prevent shorting. Keep metallic components, connectors, copper traces, internal layers, and ground planes away from the antenna area in 3D space!

3.2.2 BR-LE4.0-D2A (With Antenna)



Note: The module requires an RF ground plane on the rest of the Printed Circuit Board (PCB) area. This can be located on any layer of the PCB. Extend the RF ground plane parallel to module pins 31 and 32 the entire length of your board. Connect all ground pins and do not notch the ground plane around the module. Bottom of module is grounded so be careful of vias or conductive traces located under the modules that are not soldered masked to prevent shorting. Keep metallic components, connectors, copper traces, internal layers, and ground planes away from the antenna area in 3D space!

3.3 Module Common Hardware Details

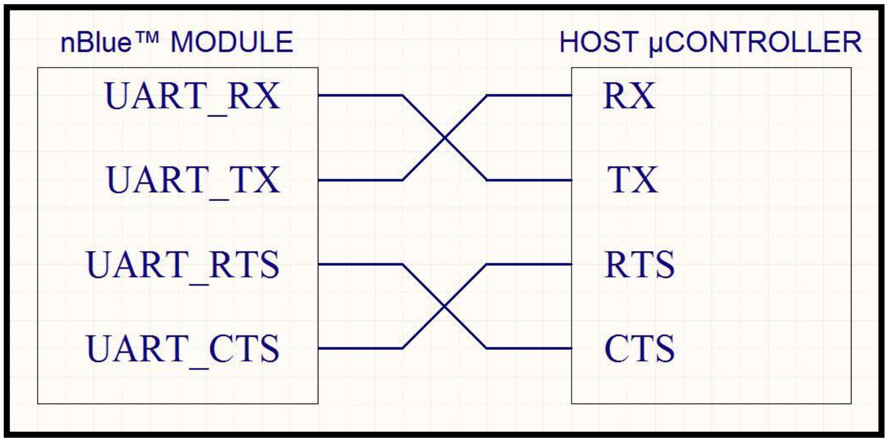
The information in this section applies to all *n*Blue modules: BR-LE4.0-S2, BR-LE4.0-S3, and BR-LE4.0-D2.

3.3.1 Power-up and Reset

There are no strict requirements for power up timing. To reset the module, the RESET line must be pulsed low for at least 1µS.

3.3.2 UART

UART_TX, UART_RX, UART_RTS and UART_CTS form a conventional asynchronous serial data port. Two-way hardware flow control is implemented by UART_RTS and UART_CTS. These signals operate according to normal industry convention. The signaling levels are nominal 0V and VDD and are inverted with respect to the signaling on an RS232 cable.



3.3.3 PIO_14 Firmware Update Mode Trigger

PIO_14 can be used to manually put the module into firmware update mode, which allows it's firmware to be updated via the UART using the *n*Blue Programmer (*n*BP) applicaion. This can be done by setting it to VDD during power up or reset and holding it at VDD until the "nBoot" message is sent from the UART.

*n*Blue Programmer (*n*BP) is a Windows application that allows firmware to be updated on all *n*Blue *Bluetooth* 4.0 modules. Updates can be performed through the module's UART interface on all modules and Over the Air (OTA) through a BLE connection on Single Mode modules (see the OTA updates section for additional requirements.) See the *n*Blue Programmer User's Guide for detailed information.

This functionality is not built into the hardware, but provided by the nBoot bootloader programmed into the module by *Blue*Radios. If the bootloader is erased using a debugger, PIO_14 will no longer trigger firmware update mode. See the Important notes section for more information.

3.4 BR-LE4.0-S2 Single Mode Module Hardware Details

The BR-LE4.0-S2 (S2) utilizes the Texas Instruments CC2540F256 SoC. For detailed specifications see the CC2540 datasheet: **http://focus.ti.com/lit/ds/symlink/cc2540.pdf**

3.4.1 S2 Operating Conditions Summary

Item	Specifications
Supply voltage (VDD)	2.0-3.6 V, 3.0 V is recommended
VDD ripple	100 mV Max
Max voltage on any pin	VDD + .3 V
Ambient Temperature Range	-40 – 85 °C

3.4.2 S2 PIO Specifications Summary

Measurements done at TA = 25°C, VDD = 3 V

Item	Specifications
Max logic low input voltage	.5 V (±50 nA current)
Min logic high input voltage	VDD - .5 V (±50 nA current)
Max logic low output voltage	.5 V
Min logic high output voltage	2.4 V
PIO drive capability	4 mA / 20 mA (PIO_2/PIO_5)
PIO internal pullup/pulldown resistors	20 kΩ

3.4.3 S2 Current Consumption Summary

For information on calculating application specific current consumption data, see:
http://www.ti.com/general/docs/litabsmultiplefilelist.tsp?literatureNumber=swra347a

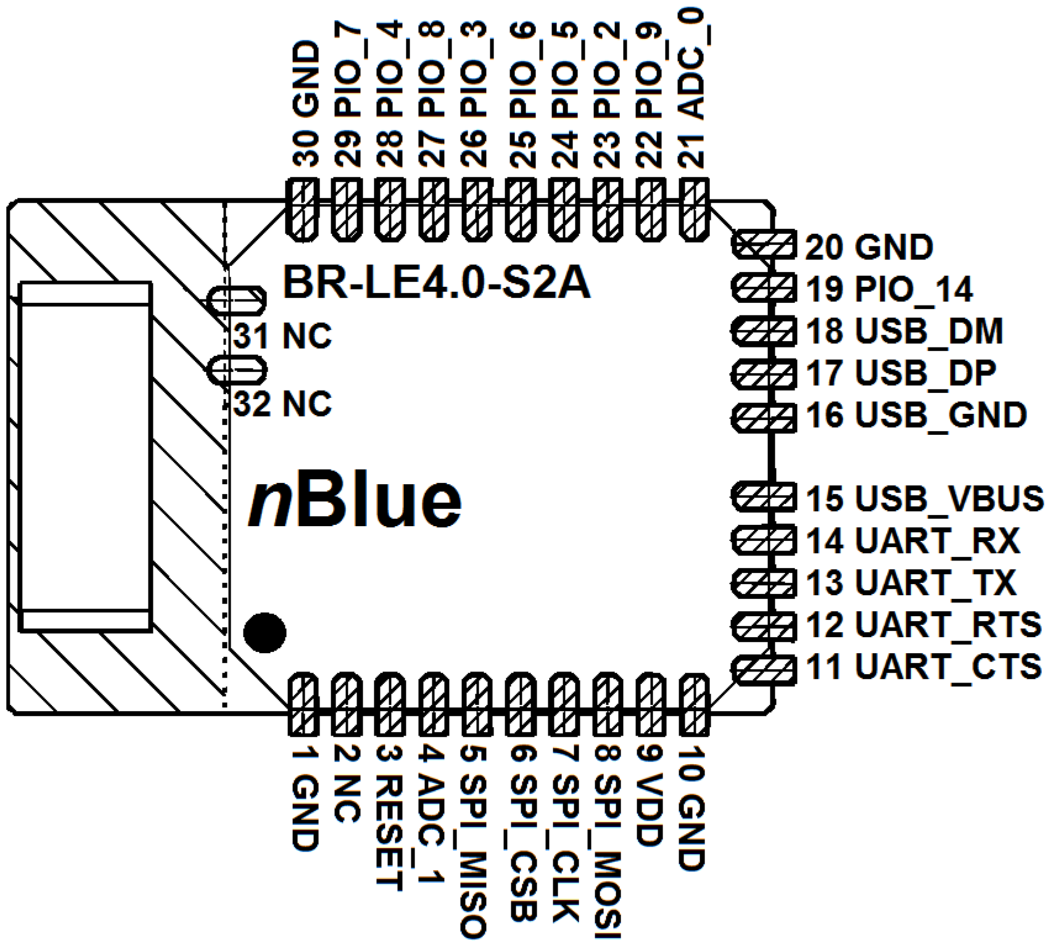
Measurements done at TA = 25°C, VDD = 3 V on BR-LE4.0-S2A running AT.s 1.2.1.3.1.0

Item	Specifications
Power Modes	
Power Mode 3 (120µs Wake-Up) AT.s in idle state with sleep mode enabled.	0.4 µA
Power Mode 2 (120µs Wake-Up) AT.s not in idle state with sleep mode enabled, this current level will be seen in between RF activity.	1.1 µA
Power Mode 1 (4µs Wake-Up)	235 µA
Idle	2.7 mA
Active AT.s in idle state.	8.1 mA
Peak RF Consumption	
RX Standard Gain	21.3 mA
RX High Gain	23.8 mA
TX -23 dBm	23 mA
TX -6 dBm	25.8 mA
TX 0 dBm	29.5 mA
TX 4 dBm	33.9 mA

3.4.4 S2 RF Specifications Summary

Item	Specifications
Frequency	2402 – 2480 MHz in 2 Mhz steps
Data Rate and Modulation	1 Mbps, GFSK
Number of Channels	40: 37 data / 3 advertising (0,12,39)
Receive Sensitivity (w/chip antenna)	-95/-89 dBm
Output Power	-23 to 4 dBm
Link Budget	Up to 99dB
RX/TX Turnaround	150 us

3.4.5 S2 Pinout



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3.4.6 S2 Pin Descriptions / PIO Map

Pin	Pin Name	CC2540 Pin	Description / Alt Functions
1	GND	-	Ground
2	NC	-	No Connect
3	RESET	-	Active-low reset
4	ADC_1	P0_1	PIO_1 / ADC Input 1
5	SPI_MISO	P0_2	PIO_10 / USART0 SPI Master In Slave Out / ADC Input 2
6	SPI_CSB	P0_4	PIO_11 / USART0 SPI Chip Select / ADC Input 4
7	SPI_CLK	P0_5	PIO_12 / USART0 SPI Clock / ADC Input 5
8	SPI_MOSI	P0_3	PIO_13 / USART0 SPI Master Out Slave In / ADC Input 3
9	VDD	-	2.0-3.6V
10	GND	-	Ground
11	UART_CTS	P1_4	USART1 CTS / PIO_15
12	UART_RTS	P1_5	USART1 RTS / PIO_16
13	UART_TX	P1_6	USART1 Transmit / PIO_17
14	UART_RX	P1_7	USART1 Receive / PIO_18
15	USB_VBUS	DVDD_USB	-
16	USB_GND	DGND_USB	-
17	USB_DP	USB_P	-
18	USB_DM	USB_N	-
19	PIO_14	P2_0	PIO_14 / ADC Trigger / nBoot FW Update Mode Trigger
20	GND	-	Ground
21	ADC_0	P0_0	PIO_0 / ADC Input 0
22	PIO_9	P1_3	PIO_9
23	PIO_2	P1_0	PIO_2
24	PIO_5	P1_1	PIO_5
25	PIO_6	P0_7	PIO_6 / ADC Input 7
26	PIO_3	P0_6	PIO_3
27	PIO_8	P1_2	PIO_8
28	PIO_4	P2_1	PIO_4
29	PIO_7	P2_2	PIO_7 / DC
30	GND	-	Ground
31	NC	-	RF Test Antenna
32	NC	-	RF Test Ground

3.5 BR-LE4.0-S3 Single Mode Module Hardware Details

The BR-LE4.0-S3 (S3) utilizes the Texas Instruments CC2541F256 SoC. For detailed specifications see the CC2541 datasheet: http://focus.ti.com/lit/ds/symlink/cc2541.pdf

The S3 is pin for pin compatible with the S2 with the exception of I2C lines replacing the USB lines of the S2. In addition, the S3 provides lower RF current consumption, better receive sensitivity (-96 vs -95 dBm), but a lower maximum output power (0 vs 4dBm) than the S2.

Measurements done at TA = 25°C, VDD = 3 V.

3.5.1 S3 Operating Conditions Summary

Item	Specifications
Supply voltage (VDD)	2.0-3.6 V, 3.0 V is recommended
VDD ripple	100 mV Max
Max voltage on any pin	VDD + .3 V
Ambient Temperature Range	-40 – 85 °C

3.5.2 S3 PIO Specifications Summary

Measurements done at TA = 25°C, VDD = 3 V

Item	Specifications
Max logic low input voltage	.5 V (±50 nA current)
Min logic high input voltage	VDD - .5 V (±50 nA current)
Max logic low output voltage	.5 V
Min logic high output voltage	2.4 V
PIO drive capability	4 mA / 20 mA (PIO_2/PIO_5)
PIO internal pullup/pulldown resistors	20 kΩ

3.5.3 S3 Current Consumption Summary

For information on calculating application specific current consumption data, see:
http://www.ti.com/general/docs/litabsmultiplefilelist.tsp?literatureNumber=swra347a

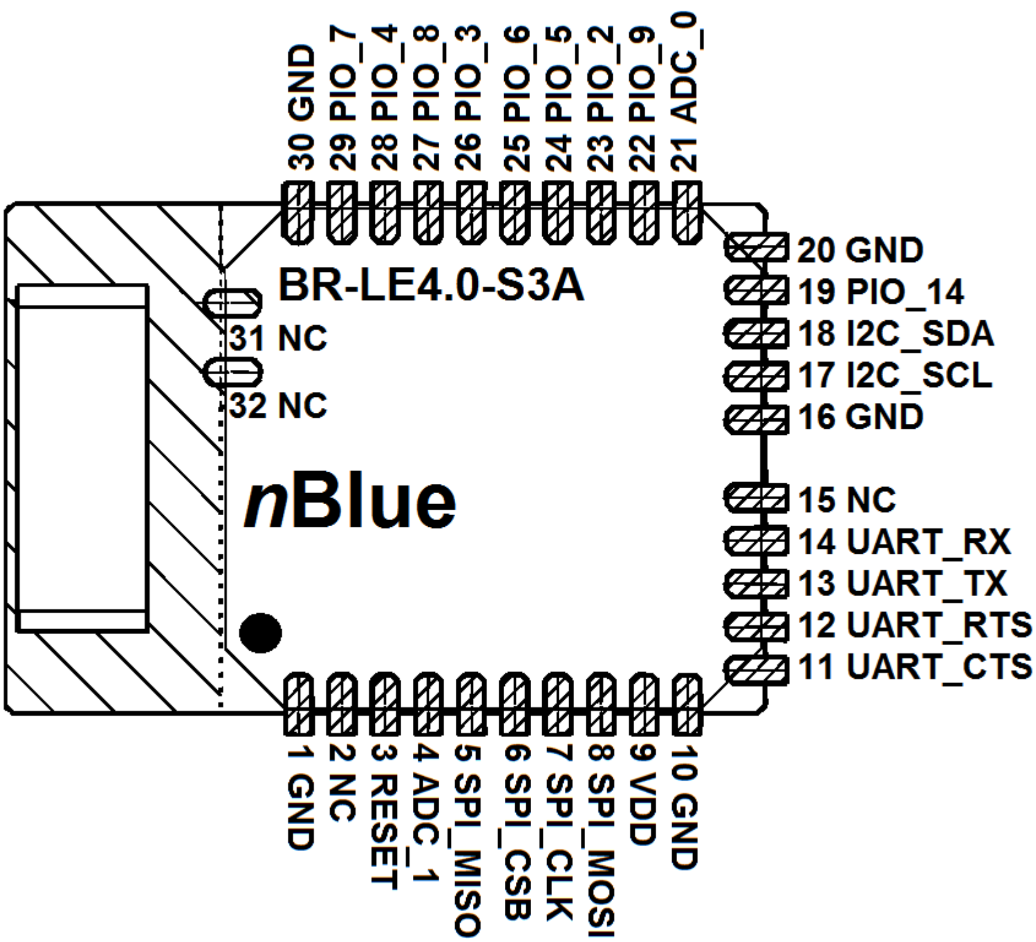
Measurements done at TA = 25°C, VDD = 3 V on BR-LE4.0-S3A running AT.s 1.2.1.3.1.0

Item	Specifications
Power Modes	
Power Mode 3 (120µs Wake-Up) AT.s in idle state with sleep mode enabled.	0.4 µA
Power Mode 2 (120µs Wake-Up) AT.s not in idle state with sleep mode enabled, this current level will be seen in between RF activity.	1.1 µA
Power Mode 1 (4µs Wake-Up)	270 µA
Idle	2.7 mA
Active AT.s in idle state.	8.1 mA
Peak RF Consumption	
RX Standard Gain	20.4 mA
RX High Gain	22.8 mA
TX -23 dBm	19.1 mA
TX -6 dBm	19.7 mA
TX 0 dBm	20.5 mA

3.5.4 S3 RF Specifications Summary

Item	Specifications
Frequency	2402 – 2480 MHz in 2 Mhz steps
Data Rate and Modulation	1 Mbps, GFSK
Number of Channels	40: 37 data / 3 advertising (0,12,39)
Receive Sensitivity (w/chip antenna)	-96/-90 dBm
Output Power	-23 to 0 dBm
Link Budget	Up to 96dB
RX/TX Turnaround	150 us

3.5.5 S3 Pinout



3.5.6 S3 Pin Descriptions / PIO Map

Pin	Pin Name	CC2541 Pin	Description / Alt Functions
1	GND	-	Ground
2	NC	-	No Connect
3	RESET	-	Active-low reset
4	ADC_1	P0_1	PIO_1 / ADC Input 1
5	SPI_MISO	P0_2	PIO_10 / USART0 SPI Master In Slave Out / ADC Input 2
6	SPI_CSB	P0_4	PIO_11 / USART0 SPI Chip Select / ADC Input 4
7	SPI_CLK	P0_5	PIO_12 / USART0 SPI Clock / ADC Input 5
8	SPI_MOSI	P0_3	PIO_13 / USART0 SPI Master Out Slave In / ADC Input 3
9	VDD	-	2.0-3.6V
10	GND	-	Ground
11	UART_CTS	P1_4	USART1 CTS / PIO_15
12	UART_RTS	P1_5	USART1 RTS / PIO_16
13	UART_TX	P1_6	USART1 Transmit / PIO_17
14	UART_RX	P1_7	USART1 Receive / PIO_18
15	NC	-	No Connect
16	GND	-	Ground
17	I2C_SCL	SCL	I2C Clock
18	I2C_SDA	SDA	I2C Data
19	PIO_14	P2_0	PIO_14 / ADC Trigger / nBoot FW Update Mode Trigger
20	GND	-	Ground
21	ADC_0	P0_0	PIO_0 / ADC Input 0
22	PIO_9	P1_3	PIO_9
23	PIO_2	P1_0	PIO_2
24	PIO_5	P1_1	PIO_5
25	PIO_6	P0_7	PIO_6 / ADC Input 7
26	PIO_3	P0_6	PIO_3
27	PIO_8	P1_2	PIO_8
28	PIO_4	P2_1	PIO_4
29	PIO_7	P2_2	PIO_7 / DC
30	GND	-	Ground
31	NC	-	RF Test Antenna
32	NC	-	RF Test Ground

3.6 BR-LE4.0-D2 Dual Mode Module Hardware Details

The BR-LE4.0-D2 utilizes the Texas Instruments MSP4305438A microcontroller and CC2564 baseband. For detailed specifications see the MSP4305438A datasheet: **http://www.ti.com/lit/ds/symlink/msp430f5438a.pdf** and the CC2564 datasheet: **http://www.ti.com/lit/ds/symlink/cc2564.pdf**

3.6.1 D2 Operating Conditions Summary

Item	Specifications
Supply voltage (VDD)	2.4-3.6 V, 3.0 V is recommended
VDD ripple	100 mV Max
Max voltage on any pin	VDD + .3 V
Ambient Temperature Range	-40 – 85 °C

3.6.2 D2 PIO Specifications Summary

- Inputs – Schmitt Trigger

Parameter	VDD	MIN	MAX	UNIT
V_{IT+} Positive-going input threshold Voltage	3	1.50	2.10	V
V_{IT-} Negative-going input threshold Voltage	3	0.75	1.65	V
V_{hys} Input Voltage hysteresis (V_{IT+} - V_{IT-})	3	0.4	1.0	V

- Outputs – General Purpose I/O (Full Drive Strength)

Parameter	Test Conditions	VDD	MIN	MAX	UNIT
V_{OH} High-Level output voltage	$I_{(OHmax)}$ = -5 mA(1)	3	VDD-0.25	VDD	V
	$I_{(OHmax)}$ = -15 mA(2)	3	VDD-0.60	VDD	V
V_{OL} Low-level output voltage	$I_{(OLmax)}$ = 5 mA(1)	3	VSS	VSS + 0.25	V
	$I_{(OLmax)}$ = 5 mA(2)	3	VSS	VSS + 0.60	V

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs should not exceed ±100 mA to hold the maximum voltage drop specified.

- Outputs – General Purpose I/O (Reduced Drive Strength)

Parameter	Test Conditions	VDD	MIN	MAX	UNIT
V_{OH} High-Level output voltage	$I_{(OHmax)}$ = -2 mA(2)	3	VDD-0.25	VDD	V
	$I_{(OHmax)}$ = -6 mA(3)	3	VDD-0.60	VDD	V
V_{OL} Low-level output voltage	$I_{(OLmax)}$ = 2 mA(2)	3	VSS	VSS + 0.25	V
	$I_{(OLmax)}$ = 6 mA(3)	3	VSS	VSS + 0.60	V

(1) Selecting reduced drive strength may reduce EMI.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs should not exceed ±48 mA to hold the maximum voltage drop specified.
(3) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs should not exceed ±100 mA to hold the maximum voltage drop specified.

3.6.4 D2 Current Consumption Summary

For information on calculating application specific current consumption data, see:
http://www.ti.com/general/docs/litabsmultiplefilelist.tsp?literatureNumber=swra347a

Measurements done at TA = 25°C, VDD = 3 V on BR-LE4.0-D2A running AT.s 3.3.0.0-D2

Item	Specifications
Power Modes	
Power Mode 3 (5µs Wake-Up) AT.s in idle state with sleep mode enabled (MSP in LPM3).	90 µA
Active AT.s in idle state (MSP in LPM0).	590 µA
Peak RF Consumption	
RX	38.5 mA
TX -23 dBm	28.5 mA
TX -6 dBm	32.0 mA
TX 0 dBm	36.5 mA
TX 4 dBm	40.0 mA
TX 10 dBm	72.0 mA

3.6.5 D2 RF Specifications Summary

- General

Item	Specifications
Receive Sensitivity (w/chip antenna)	-95 dBm
Output Power	10.5 dBm max
Link Budget	Up to 105.5 dB
RX/TX Turnaround	150 us

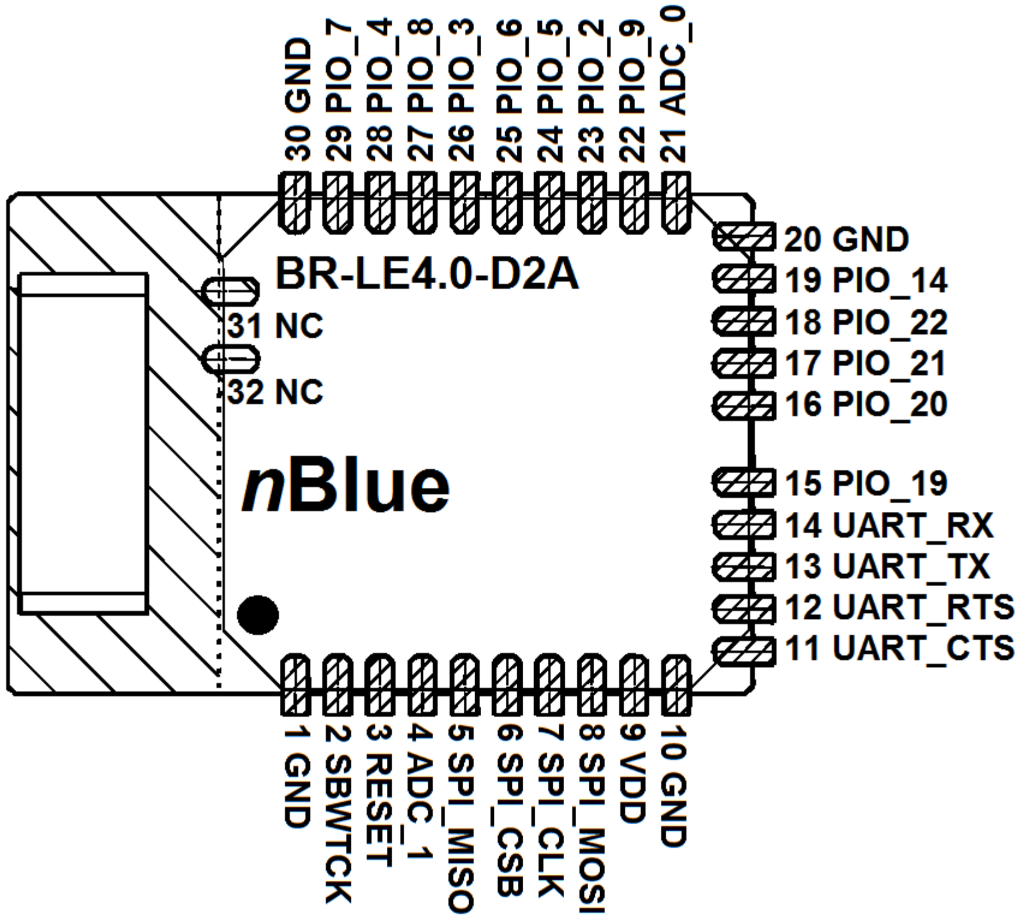
- Classic Bluetooth

Item	Specifications
Frequency	2402 – 2480 MHz in 1 Mhz steps
Data Rate and Modulation	BR:1 Mbps, GFSK / EDR: 2-3 Mbps PSK
Number of Channels	79

- Bluetooth Low Energy

Item	Specifications
Frequency	2402 - 2480 MHz in 2 Mhz steps
Data Rate and Modulation	1 Mbps, GFSK
Number of Channels	40: 37 data / 3 advertising (0,12,39)

3.6.6 D2 Pinout



3.6.7 D2 Pin Descriptions / PIO Map

Pin	Pin Name	MSP430 Pin	Description / Alt Functions
1	GND	GND	Ground
2	TEST/ SBWTCK	TEST/ SBWTCK	Test mode pin – Selects four wire JTAG operation, Spy-Bi-Wire input clock when Spy-Bi-Wire operation activated
3	RESET	RST	Reset input active low (47K pullup internal) I/O Non-maskable interrupt input, Spy-Bi-Wire data input/output when Spy-Bi-Wire operation activated.
4	ADC_1 (PIO_1)	P6.1	General-purpose digital I/O, Analog input A1 – ADC
5	SPI MISO (PIO_10)	P3.2	General-purpose digital I/O, Slave out, master in – USCI_B0 SPI mode, I2C clock – USCI_B0 I2C mode
6	SPI CS (PIO_11)	P3.0	General-purpose digital I/O, Slave transmit enable – USCI_B0 SPI mode
7	SPI CLK (PIO_12)	P3.3	General-purpose digital I/O, Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode
8	SPI MOSI (PIO_13)	P3.1	General-purpose digital I/O, Slave in, master out – USCI_B0 SPI mode, I2C data – USCI_B0 I2C mode
9	VDD		2.4-3.6 V
10	GND		Ground
11	UART0 CTS (PIO_15)	P2.1	General-purpose digital I/O with port interrupt, TA1 CCR0 capture: CCI0A input, compare: Out0 output
12	UART0 RTS (PIO_16)	P2.0	General-purpose digital I/O with port interrupt, TA1 clock signal TA1CLK input, MCLK output
13	UART0 TX (PIO_17)	P10.4	General-purpose digital I/O, Transmit data – USCI_A3 UART mode,
14	UART0 RX (PIO_18)	P10.5	General-purpose digital I/O, Receive data – USCI_A3 UART mode,
15	PIO_19	P5.6	General-purpose digital I/O, Transmit data – USCI_A1 UART mode, Slave in, master out – USCI_A1 SPI mode
16	PIO_20	P5.7	General-purpose digital I/O, Receive data – USCI_A1 UART mode, Slave out, master in – USCI_A1 SPI mode
17	PIO_21	P3.6	General-purpose digital I/O, Clock signal input – USCI_A1 SPI slave mode, Clock signal output – USCI_A1 SPI master mode
18	PIO_22	P5.5	General-purpose digital I/O, Slave transmit enable – USCI_A1 SPI mode
19	PIO_14	P6.6	General-purpose digital I/O, Analog input A6 – ADC, nBoot FW Update Mode Trigger
20	GND		Ground
21	ADC_0 (PIO_0)	P6.0	General-purpose digital I/O, Analog input A0 – ADC
22	PIO_9	P5.0	General-purpose digital I/O, Analog input A8 – ADC, Output of reference voltage to the ADC,

			Input for an external reference voltage to the ADC
23	PIO_2	P1.1	General-purpose digital I/O with port interrupt, TA0 CCR0 capture: CCI0A input, compare: Out0 output, BSL transmit output
24	PIO_5	P1.5	General-purpose digital I/O with port interrupt, TA0 CCR4 capture: CCI4A input, compare: Out4 output
25	PIO_6	P1.6	General-purpose digital I/O with port interrupt, SMCLK output
26	PIO_3	P1.0	General-purpose digital I/O with port interrupt, TA0 clock signal TACLK input, ACLK output (divided by 1, 2, 4, or 8)
27	PIO_8	P5.1	General-purpose digital I/O, Analog input A9 – ADC, Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
28	PIO_4	P1.2	General-purpose digital I/O with port interrupt, TA0 CCR1 capture: CCI1A input, compare: Out1 output, BSL receive input
29	PIO_7	P6.7	General-purpose digital I/O,Analog input A7 – ADC
30	GND	-	Ground
31	NC	-	RF Test Antenna
32	NC	-	RF Test Ground

4 Programming/Debugging

A debugger is only needed for debugging custom embedded applications through an IDE. A debugger is not necessary for updating firmware on modules using the AT.s command set or for programming modules with custom firmware.

4.1 nBlue Programmer

***n*Blue™ Programmer** (*n*BP) is a Windows application that allows firmware to be updated on all ***Blue*Radios®** ***n*Blue™** *Bluetooth* 4.0 modules. Updates can be performed through the module's UART interface on all modules and Over the Air (OTA) through a BLE connection on Single Mode modules.

Flow control is not used by *n*BP, so only RX,TX,VCC and GND are needed to update the firmware through the UART. ***n*BP does not use the CC Debugger DD/DC lines on the S2 or the SPY-Bi Wire interface on the D2.**

All *n*Blue modules come programmed with a bootloader (*n*Boot), to enable firmware updates via *n*Blue Programmer (*n*BP), and a *Blue*Radios IEEE address. These elements are stored in flash and can be accidentally erased using a debugger. Once they have been erased they cannot be reprogrammed by a client, it is a factory process only. When the *Blue*Radios IEEE address is erased, the TI IEEE address stored in ROM will be used.

To protect *Blue*Radios IP, any firmware distributed by *Blue*Radios or firmware built using libraries distributed by *Blue*Radios will not run without the presence of the nBoot bootloader. This means *Blue*Radios firmware will no longer run once the bootloader has been erased. At this point the module can only be programmed with custom firmware.

For security purposes, after the bootloader is programmed into BR-LE4.0-SX modules during production the debug interface is locked. In order to program a module using a CC Debugger it will then need to be unlocked, which will erase the entire flash including the module's bootloader and IEEE address, making it incapable of performing firmware updates using *n*BP. For this reason, single mode BR-LE4.0-SX firmware updates should only be performed using *n*BP, not a CC Debugger. Custom software can still be flashed using *n*BP, see the *n*Blue Programmer User's Guide for more information.

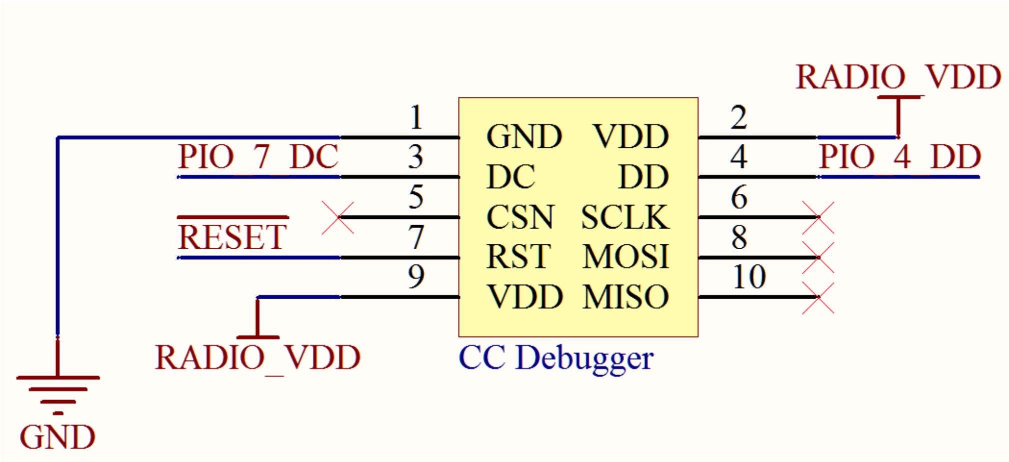
On BR-LE4.0-D2 modules the bootloader is locked separately from the program flash in the MSP430's BSL flash, so firmware can safely be loaded into the D2 through a debugger without erasing the bootloader.

See the nBlue Programmer User's Guide for more information.

4.2 CC Debugger for BR-LE4.0-SX Single Mode Modules

PIO_4 and PIO_7 also function as the Debug Data (DD) and Debug Clock (DC) lines, allowing the modules to be connected to a TI CC Debugger for debugging and programming. The debug headers on the evaluation boards can be connected directly to a CC Debugger. See the CC Debugger User's Guide for more information: http://www.ti.com/tool/cc-debugger

When using a CC Debugger with any of the evaluation boards, be sure that only one power source is supplying the board at a time. Either disconnect the board from its power source before connecting the CC Debugger, or to enable debugging without disconnecting from your power source, leave pin 9 not connected or cut wire 9 on the CC Debugger cable.



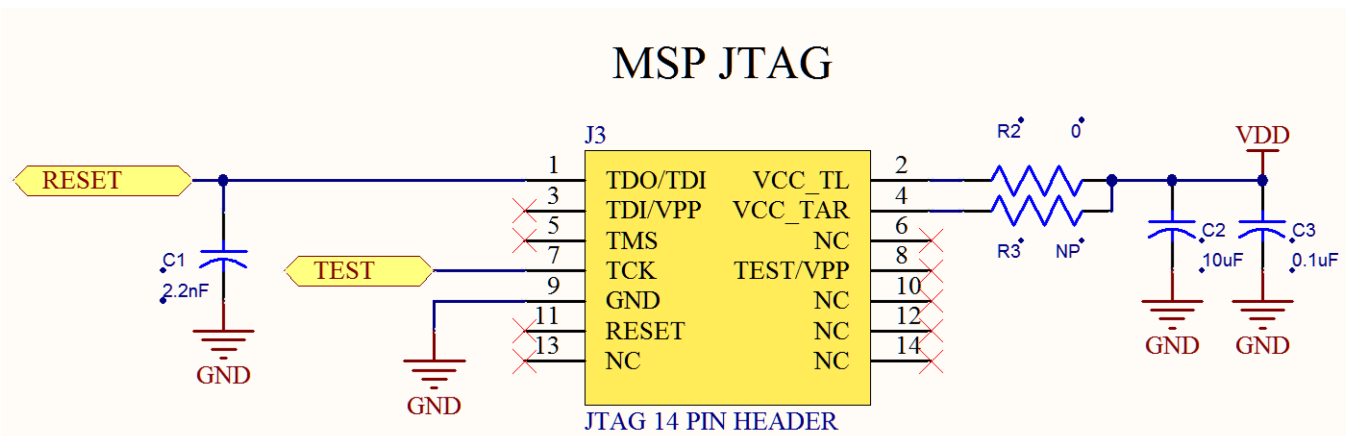
CC Debugger

4.3 BR-LE4.0-D2 Dual Mode Module Debugging

SBWTCK (TEST) and SBWTDIO (Reset) allow the module to be connected to a TI MSP-FET430UIF for debugging and programming via SPY-Bi Wire. The debug headers on the evaluation boards can be connected directly to a MSP-FET430UIF. See the MSP-FET430UIF User's Guide for more information http://www.ti.com/lit/ug/slau278j/slau278j.pdf.

The RESET pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 2.2nF. A 47K pull-up resistor on the reset line is internal to the module.

When using a Texas Instuments MSP430 USB-Debug-Interface MSP-FET430UIF Debugger with any of the *n*Blue evaluation boards, be sure to only use the MSP-FET430UIF Debugger power source.
Connect either VCC_TL to VDD to power the module from the debugger or connect VCC_TAR to VDD if the board is self-powered.



MSP-FET430UIF

5 Evaluation Boards

5.1 Drivers

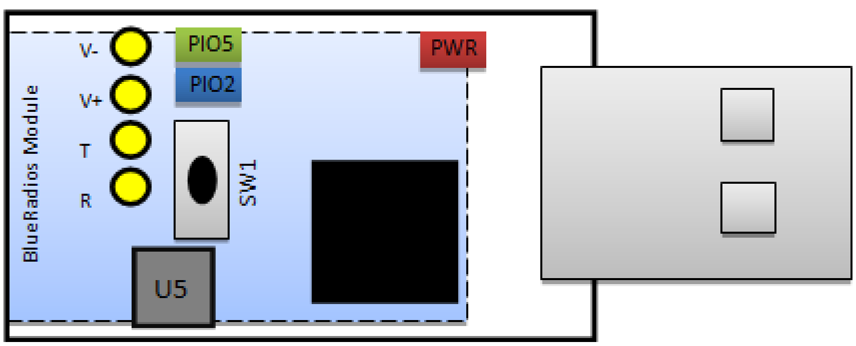
The Dongle and the DevBoard both require FTDI virtual COM port drivers to work with a host OS. If your OS doesn't automatically find them, they can be obtained from: http://www.ftdichip.com/Drivers/VCP.htm.

5.2 BR-MUSB-LE4.0 Mini Dongle

This Dongle provides users with a small, ready to use Single or Dual Mode Device. It just needs to be plugged into a USB host port and it's ready to receive AT commands. The module's UART is connected to an FTDI USB to Serial Converter and LEDs are connected to PIOs 2 and 5. If needed, the firmware can be updated by using *n*Blue Programmer.

Layout:

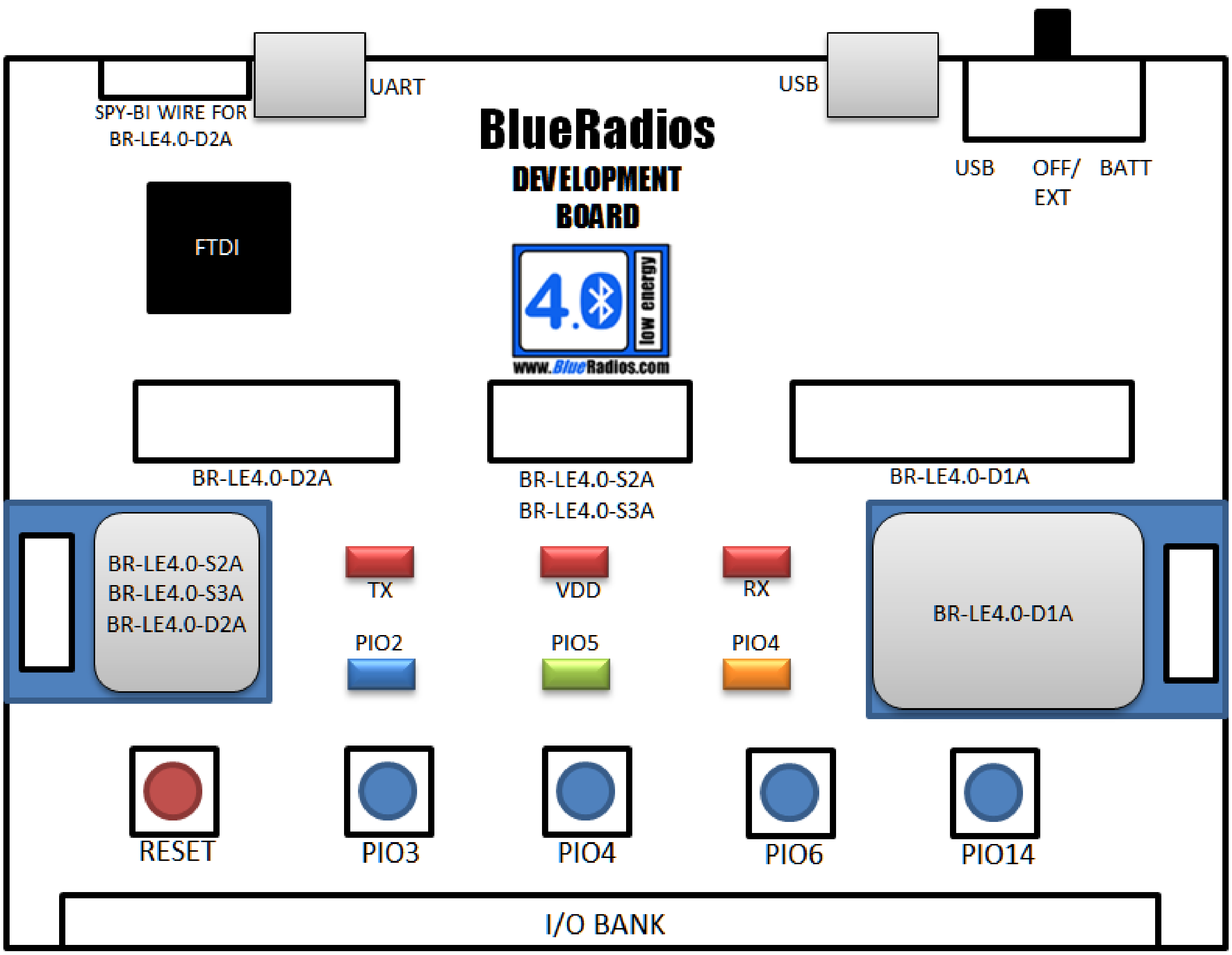
- Green LED- PIO5 Radio Status
- Blue LED – PIO2 Connection Status
- Red LED – 5V USB Power
- V- - GND (SPY-BI Wire for BR-LE4.0-D2A)
- V+ - VDD (SPY-BI Wire for BR-LE4.0-D2A)
- T – Test (SPY-BI Wire for BR-LE4.0-D2A)
- R – Reset (SPY-BI Wire for BR-LE4.0-D2A)
- FTDI – Serial to USB IC
- SW1 (optional) – Push Button, Connected to PIO4
- U5 (not populated) – Apple MIFI IC



5.3 BR-DEV-LE4.0 Development Board

The BR-DEV-LE4.0 Development Board (Dev Board) provides users with a ready to use out of the box development system that's easily customizable to fit the user's needs. This board is designed to support all of the *Blue*Radios modules. LEDs are connected to PIOs 2,4,5,TX,RX, and switches are connected to PIOs 3,4,6,14 and RESET. In addition, all of the PIOs are accessible on the I/O bank header. The Dev Board has two USB connectors, one attached to a USB to Serial Converter to provide access to the UART through a PC and the other connected to the internal USB controller on BR-LE4.0-S2 modules. It also has three programming/debugging headers to support the different processors in each module.

The module on the Dev Board can be powered by USB, 3.0V CR2032 battery, a debugger or an external supply. For powering by USB set the power switch to the USB position and connect either USB port to a host. For powering by battery set the power switch to the BATT position and insert a CR2032 into the battery holder on the bottom of the board. To power through the debug header or an external supply (2.0-3.6V), set the switch to the OFF/EXT position. An external supply can be connected to the GND and VDD signals on the I/O bank headers.



Dev Board Rev B

5.4 BR-BOB-ANT Breakout Board

The BR-BOB-ANT is an unpopulated breakout board (BOB) that can be customized to fit the user's specific needs. The user will need to solder a module on to the BOB, supply power to the BOB, and connect the UART to an external microcontroller or a PC. Test points are provided for every pin on the module and LED pads are available for PIO_2 (LED_1) and PIO_5 (Led_2). A CC Debugger header is provided, as well as an IBC_2 header.

A USB Serial Breakout Board (SBB) is available to make the BOB easier to use out the box. The SBB allows the BOB to be plugged into a USB host port for testing. The SBB will supply 3.3V to the BOB, so no external power supply is needed. It can be wired to the BOB as seen in the diagram below: